readyRM

Data (the Address in SDRAM)

*Display Control*

VESA

data

16 bits in 1 clk

RAM Manager : responsible for the Ras/Cas/Burst of the SDRAM which denoted by the RAM

SDRAM

WBM

Ras/Cas/Burst

FIFO\_A

FIFO\_B

FIFO\_COTROL

Responsible for the toggling between the 2 FIFOs

\*Careful with filling one FIFO before the VESA finishes reading from the other.

RAM

AddRAM

DataRAM

Opcode decoder

If opcode[26..29]=[1 1 1 1]

Then readyRM = 1

valid

valid

[0..31]

Opcode FIFO

[0..31]

Opcode unite

wbs

[0..7]

AddRAM=20x+y